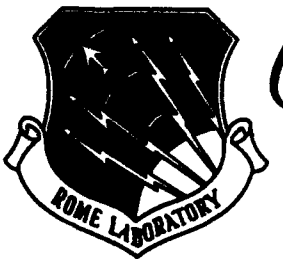
RL-TR-92-106
Final Technical Report
May 1992



VLSI DESIGN FOR RELIABILITY - HOT ELECTRON

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REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. AGENCY USE ONLY (Leave Blank)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	May 1992	Final Mar 90 - Mar 91

4. TITLE AND SUBTITLE
VLSI DESIGN FOR RELIABILITY - HOT ELECTRON

5. FUNDING NUMBERS
C - F30602-88-D-0028
Task - N-O-5701
PE - 62702F
PR - 2338
TA - 01
WU - P2

6. AUTHOR(S) Sung-Mo Kang, Yusuf Leblebici, Ping Li, Ibrahim Hajj, Carlos Diaz, Yung-Ho Shih

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Urbanna IL 61801-3082

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
Rome Laboratory (ERDD)
Griffiss AFB NY 13441-5700

10. SPONSORING/MONITORING AGENCY REPORT NUMBER
RL-TR-92-106

11. SUPPLEMENTARY NOTES
Rome Laboratory Project Engineer: Martin J. Walter/ERDD(315) 330-4102

12a. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution unlimited.

12b. DISTRIBUTION CODE

13. ABSTRACT (Maximum 200 words)

This report describes the accomplishments during the contract period (March 27, 1990 to March 26, 1991) on the computer-aided analysis of CMOS device and circuit degradation due to hot-electron effects. The task involved four subtasks: (1) modeling of the gate oxide degradation in n-channel MOS transistor; (2) modeling of n-channel MOS transistor behavior with localized oxide damage; (3) simulation of gate oxide degradation during long-term circuit operation; (4) determination of overall circuit performance after hot-electron stress. For the modeling of the gate oxide degradation in nMOS transistor, a localized triangular charged density distribution function has been introduced in the drain end of the channel. This model was effective in explaining the local electric potential near the drain, especially on the flatband voltage and also the changes in the local channel electron mobility. To model the behavior of nMOS transistor with local oxide damages, a new one-dimensional I-V equation has been derived and implemented in a generic circuit simulator, iSMILE program. For the modeling of gate oxide degradation process, the rate equations governing the generation of interface states have been implemented for dynamic circuit operating conditions. With these mechanisms implemented, the iSMILE program has been able to simulate the degradation of circuit performances dynamically. For large scale reliability simulation, simpler models have been devised and used in the iDSIM2 program.

14. SUBJECT TERMS	15. NUMBER OF PAGES
Hot electron degradation, Circuit modeling, Design for Reliability	50
	16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED	U/L

FINAL REPORT EVALUATION
Contract F30602-88-D-0028 Task N-0-5701
VLSI Design For Reliability - Hot Electrons

The growth in the use of custom, semi-custom, and application specific ICs (ASICs) in AF systems has brought several changes to the reliability qualification process. This occurred because the costs associated with reliability characterization have become a major part of the device cost when there are only a few hundred or thousand of such devices produced. Further, the cost of a second or third pass at the design/fabricate/test/evaluate reliability cycle is very time consuming as well as expensive.

Analyzing an IC design for susceptibility to life limiting failure mechanisms is one approach to enhance the probability that at the end of the first pass of the design/fabricate/test/evaluate reliability cycle, the device will have an acceptable reliability.

This effort addresses the development of simulation methods for hot electron degradation in CMOS ICs. It uses a realistic charge distribution in the gate oxide to successfully explain the local flat band voltage, electric potential near the drain, and the channel electron mobility. A one dimensional model suitable for LSI circuit analysis has been developed and applied to the simulation of a circuit with several hundred transistors. Future work will include extending this modeling effort into a macromodeling scheme to address circuits with 10K to 100K transistors.

Other efforts being sponsored by Rome Lab in the area of design analysis for ICs address the estimation of current and current density from statistical simulations. These estimations are being applied to the analysis of the susceptibility of the design to electromigration and short term design concerns such as IR drop and ground bounce in the power and ground busses.

MARTIN J. WALTER
Project Engineer
RL/ERDD

VLSI DESIGN FOR
RELIABILITY-HOT ELECTRON

Final Report

Account No. 93928-30/Order No. RI-68909X

Contract F30602-88-D-0028(Task N-0-5701)

I. Introduction

Long-term reliability of MOS VLSI circuits is becoming an important issue as the density of VLSI chips increases with shrinking design rules. In the conventional computer-aided design approach, physical aging of integrated circuit elements due to degradation mechanisms has been a secondary concern, and the qualification of circuit reliability has been accomplished only by accelerated burn-in tests after manufacture. This approach has several drawbacks with respect to translating the reliability data into physical design improvements for long-term reliability of the circuit. First, the repetition of the "design-manufacture-test" cycle for incremental reliability improvements is prohibitively expensive in most small-volume productions. Moreover, some of the long-term degradation mechanisms cannot be correctly identified by accelerated burn-in tests. As a result, the efforts to improve the long-term reliability of MOS VLSI circuits have been focused on process and technology modifications, rather than design modifications of the circuit. The development and use of accurate reliability simulation tools is therefore crucial for early assessment and improvement of circuit reliability.

The hot-carrier induced degradation of MOS transistor characteristics is one of the primary mechanisms affecting the long-term reliability of MOS VLSI circuits. It is likely to become even more critical in the future-generation chips, since the scaling of transistor dimensions without a corresponding scaling of the power supply voltage (so called constant-voltage

scaling) aggravates this problem [1],[2]. The hot-carrier induced degradation of MOS transistors is caused by the injection of high-energy electrons and holes into the gate oxide region near the drain. The "damage" is in the form of localized oxide charge trapping and/or interface trap generation, which gradually builds up and permanently changes the oxide-interface charge distribution [3],[4]. The extent of the hot-carrier damage each transistor experiences is determined by its terminal voltage waveforms, i.e., by the operating conditions of the circuit. Consequently, the mechanism of hot-carrier induced device degradation must be examined within the context of circuit simulation.

The performance degradation in the devices leads to the degradation of circuit performance over time. The reliability simulation should determine how the overall circuit performance is affected as a result of device aging, and which devices are most likely to cause critical circuit performance failures. The framework of a hot-carrier reliability simulation tool involves (i) modeling the gate oxide degradation in the MOS transistor as a function of its operating conditions, (ii) modeling the behavior of the MOS transistor with localized oxide damage, (iii) simulation of gate oxide degradation during long-term circuit operation, and (iv) determination of the overall circuit performance after hot-carrier stress. The integration of these components into a simulation framework is the prerequisite for accurate prediction of the long-term circuit reliability characteristics.

For circuit simulation purposes, the behavior of damaged transistors was represented by one-dimensional homogeneous models, based on the assumption that the oxide-interface charge is uniformly distributed over the entire channel region. In their earlier work, Hsu and Tam have shown that under the uniform charge profile assumption the amount of threshold voltage change is linearly proportional to the amount of total charge density [5]. However, even the definition of the MOSFET threshold voltage loses much of its physical meaning for a channel with nonuniform oxide charge and interface trap distribution [3]. Thus the effect of localized hot-carrier damage on the I-V characteristics of transistors cannot be accurately

accounted for by uniform device models.

The need to represent the damaged MOS transistor by a nonuniform and non-symmetrical structure has been recognized earlier [1] and several two-dimensional modeling approaches have been proposed. Haddara and Christoloveanu have presented a two-dimensional model for the locally damaged MOSFET using two channel regions and uniform charge distribution within the damaged region [6]. Schwerin *et al.* have modeled the behavior of the MOS transistor with fixed oxide charges as well as with fast interface states located near the drain using the 2-D device simulator MINIMOS 3 [7]. Their simulation results have shown that the fast interface states are necessary for accurate modeling of the subthreshold current. The nonuniform fixed oxide charge model has also been implemented by Roblin *et al.* for the 2-D device simulator PISCES [8].

Although two-dimensional device simulation can accurately represent the effect of localized hot-carrier damage on the I-V characteristics, it cannot be applied efficiently to simulate circuits with a large number of transistors. For efficient circuit-level simulation, a one-dimensional device model capable of representing the linear region operation of the damaged nMOS transistor has been proposed earlier by the authors [9]. In this project, a new one-dimensional model is developd for nMOS transistors with hot-carrier induced oxide damage. This MOSFET model accounts for the localization of the oxide damage near the drain by using a realistic charge density distribution profile. It is capable of accurately representing the observed behavior of the locally damaged transistor both in the linear and the saturation regions, a task which could not be accomplished using previous one-dimensional models with uniform oxide charge distribution [10]. The derivation of the model is consistent with the well-known gradual channel approximation theory. The model has been implemented in the circuit simulation program iSMILE [11] to enable efficient reliability simulation of CMOS circuits. The model representation of the hot-carrier induced oxide damage is discussed and the underlying assumptions for the transistor model are presented in Section II. The analytical

derivation of the drain current model is given in Section III, including the modification of the model to account for channel velocity limitations in short-channel devices. The application of a pseudo-two-dimensional approach to the modeling of damaged nMOS transistors will also be discussed. The accuracy of the new model will be demonstrated in Section V by comparing the simulation results with experimental data. The simulation of hot-carrier induced device degradation upon circuit performance are investigated in Section IV using the iSMILE circuit simulator and iDSIM program. The conclusions will be summarized in Section V.

II. Hot-Carrier Induced Gate Oxide Degradation

A thorough understanding of the processes which are responsible for the long-term degradation of device characteristics is naturally the first prerequisite for building accurate simulation models, and for evaluating the device-level and circuit-level damages associated with these processes.

The hot-carrier induced damage in nMOS transistors is assumed to result either in trapping of carriers on defect sites in the oxide or the creation of interface states at the silicon-oxide interface, or both. Recent studies have shown that the charge-pumping technique can provide precise and direct information on the interface properties in MOS transistors [3],[12]. In addition, this technique is capable of independently providing the amount of interface traps generated during injection, and the amount of charges that have been trapped in the gate oxide, even for the case of localized degradation.

Two distinct voltage regions of stressing have been identified which indicate different types of degradation. For the region of maximum substrate current ($V_{DS} \approx 2 \cdot V_{GS}$), the oxide damage has been linked to interface trap generation through hot-electrons and hot-holes, and no significant charge trapping could be observed [2]-[4]. For the region of high electron injection into the oxide ($V_{DS} \approx V_{GS}$), the damage is caused to a great extent by charge trapping, and also by moderate interface trap generation [4],[8]. Consequently, an investigation of hot carrier induced degradation mechanisms must encompass the charge trapping and the

interface trap generation in nMOS transistors, both of which are caused by hot-carriers injected into the gate oxide.

A. Charge Trapping

When the transistor is operating in or near the saturation region, the electrons moving from the source to the drain experience a significant velocity increase due to the high horizontal electric field. A small percentage of these high-energy electrons are deflected towards the gate electrode by elastic scattering. If the kinetic energy of the deflected electron (hot electron) is sufficient to overcome or tunnel through the potential energy barrier at the silicon-oxide interface, the electron is *injected* into the gate oxide near the drain. This process can be characterized by the electron injection current into the gate oxide in terms of drain current I_D and other parameters:

$$I_{EI} = \frac{1}{2} I_D \frac{t_{ox}}{\lambda_r} \left[\frac{\lambda E_m}{\Phi_b}\right]^2 P(E_{ox}) \exp\left[-\frac{\Phi_b}{E_m \lambda}\right] \quad . \tag{1}$$

Here, E_m denotes the maximum channel electric field in the direction of the channel current, Φ_b denotes the Si–SiO_2 potential barrier height and $P(E_{ox})$ denotes the probability that an electron can overcome this potential barrier. It is assumed that this injection is confined to a relatively small portion of the channel near the drain. The electron injection current reaches its peak value for $V_{GS} \approx V_{DS}$, which is identified as a bias condition favorable for charge trapping [4]. The relationship between the injected electron current and the trapped oxide charge density N_{ox} can be described by

$$N_{ox}(N_{inj}) = N_1 \left[1 - e^{-\sigma_1 N_{inj}}\right] + N_2 \left[1 - e^{-\sigma_2 N_{inj}}\right] , \tag{2}$$

where σ_1 and σ_2 represent the trapping cross-sections and the injected electron fluence N_{inj} is calculated as the integral of electron injection current density over time [9].

B. Interface Trap Generation

The other prominent hot-carrier injection mechanism is based on impact ionization, in which high-energy electrons moving horizontally along the channel create electron/hole pairs by collisions near the drain. These hot carriers have been identified as being responsible for the generation of oxide-interface states (traps), a process which is distinctly different from charge trapping. The hot-electron induced trap generation process can be characterized by the *bond-breaking current* I_{BB} [2]:

$$I_{BB} = C_1 \, I_D \exp \left[\frac{- \Phi_{it,e}}{q \, \lambda_e \, E_m} \right] \tag{3}$$

where $\Phi_{it,e}$ represents the critical energy for electrons to create interface traps, and λ_e is the mean free path for electrons. A similar expression can be derived for the hot-hole component of I_{BB}. Using the rate equations governing the generation of interface states (N_{it}), the long-term interface charge accumulation under dynamic operating conditions is described by the following simple differential equation [20].

$$\frac{dN_{it}}{dt} \left[1 + B_p \frac{X_H}{D_H} N_{it} \right] = K \langle I_{BB} \rangle \tag{4}$$

Here, $\langle I_{BB} \rangle$ represents the average value of the bond-breaking current over a period, D_H and X_H represent diffusion constants, K and B_p represent process-dependent coefficients.

The charge trapping model given by Eqs. (1) and (2), and the interface trap generation model given by Eqs. (3) and (4) can be applied for predicting the long-term dynamics of hot-carrier induced device degradation. It must be noted that the effects of hot-carrier degradation upon current-voltage characteristics of nMOS transistors cannot be explained by simple parameter changes in the conventional MOSFET simulation models. To account for the behavior of the damaged nMOS transistors using a conventional SPICE model such as the BSIM, most, if not all, of the model parameters must be modified accordingly [21]. Even such an approach would be largely empirical, since the conventional uniform MOSFET

models do not accommodate localized modifications of physical device parameters. This fact complicates the simulation of the damaged device behavior with various levels of hot-carrier damage.

The localization of hot-carrier injection into the gate oxide leads to the localization of the resulting oxide damage in the form of charge trapping and interface trap generation [3],[4],[22]. The change of oxide characteristics due to charge injection occurs in a relatively short channel section (approximate length of 0.1 μm) at the drain end. This localization of damage largely complicates the interpretation of damaged transistor characteristics, and it is also responsible for the observed asymmetry of current-voltage characteristics in damaged nMOS transistors.

Although it is quite clear that the hot-carrier induced oxide charge is localized very near to the drain, the shape of the charge distribution profile is not known exactly. The existing measurement results indicate that the peak value of the charge profile and the length of the damaged region increase with hot-carrier stress. Haddara *et al.* [6] and Roblin *et al.* [8] have used uniform (constant) charge profiles in two-dimensional device simulations, whereas Schwerin *et al.* have assumed a Gaussian charge distribution [7]. In all cases the length of the damaged region is assumed to be about 0.1 μm. Ancona *et al.* [12] have reported charge pumping measurement results which indicate a triangular charge distribution profile with a sharp peak very close to the drain (Fig. 1). For the derivation of model equations, the localized oxide-interface charge due to hot-carrier injection will be represented by a simple triangular charge density distribution profile (Fig. 2).

$$Q_{it}(y) = \begin{cases} 0 & 0 \le y < L_1 \\ \dfrac{Q_{peak}}{L_2}\,(y - L_1) & L_1 \le y < L \end{cases} \qquad (5)$$

Here, L_1 denotes the length of the undamaged channel region, whereas L_2 denotes the length of the damaged region. Notice that the amount of oxide-interface damage is described by

only two parameters, i.e., Q_{peak} and L_2. The hot-carrier induced oxide-interface charge has a significant influence on two device properties: (i) it affects the local electric potential in the adjacent drain region, and (ii) it changes the local channel electron mobility. The potential effect can be accounted for as an additional term in the flat-band voltage (V_{FB}) expression.

$$V_{FB}(y) = \Phi_{MS} - \frac{Q_{ox}}{C_{ox}} - \frac{Q_{it}(y)}{C_{ox}} \tag{6}$$

Here Φ_{MS} represents the work function difference, Q_{ox} represents the constant positive oxide-interface charge density in C/cm^2 which is independent of hot-carrier injection, and C_{ox} represents the gate oxide in F/cm^2. The reduction of channel electron mobility can be represented by Mathiessen's rule as proposed by Nishida and Sah [13]. This approach assumes that the total reciprocal mobility is composed of bulk mobility μ_0 and oxide-interface charge scattering mobility μ_{ox} as follows.

$$\frac{1}{\mu_n(y)} = \frac{1}{\mu_0} + \frac{1}{\mu_{ox}(y)} \tag{7}$$

The electron mobility due to charge scattering is given by

$$\mu_{ox}(y) = 1000\ (3\times10^{11}/Q_{it}(y))\ (T/80) \qquad [cm^2/V\cdot s] \tag{8}$$

where $Q_{it}(y)$ is the area-density of the oxide-interface charge. The derivation of drain current model equations is presented in the following section.

III. Modeling of nMOS Transistor with Gate Oxide Damages for Reliability Simulation

The drain current model derivation is based on the assumption that the gradual-channel approximation is valid for the damaged nMOS transistor. This approximation states that the electric field in the direction of current flow is much smaller than the field perpendicular to the silicon surface, thus allowing the one-dimensional analysis of the drain current I_D. Throughout this section, all voltage values will be given with respect to the source potential, unless stated otherwise. The mobile electron charge Q_n along the channel region is expressed

by

$$Q_n(y) = - C_{ox} \left[V_G - V_C(y) - V_{FB}(y) - 2|\Phi_P|\right] + \left[2\varepsilon_S q N_a (2|\Phi_P| + V_C(y) - V_B)\right]^{\frac{1}{2}} \quad (9)$$

where V_G, V_B and V_C represent the gate voltage, the substrate voltage and the channel voltage, respectively. First, the derivation will be carried out in the linear operation region, where a continuous channel is assumed to exist between the source and the drain.

A. Linear Region Equations

When the nMOS transistor is operating in the linear region, an incremental length, dy, along the channel sustains a voltage drop, dV_C, that can be expressed as the well-known product of the drain current I_D and the incremental channel resistance:

$$dV_C(y) = - I_D \frac{dy}{W \mu_n(y) Q_n(V_C, y)} \quad (10)$$

or

$$I_D \, dy = - W \mu_n(y) Q_n(y) \, dV_C \quad . \quad (11)$$

The solution of this differential equation will be substantially simplified using the following observations. First, the oxide-interface charge distribution profile $Q_{it}(y)$ is equal to zero between y=0 and $y=L_1$ according to Eq. (5). Thus the right-hand side of Eq. (11) is only a function of the channel voltage V_C in this undamaged region. To achieve a similar simplification in the damaged region of length L_2, the charge density will be assumed to be constant and equal to the *average* value of $Q_{it}(y)$ in this region, i.e., $Q_{it}=Q_{peak}/2$. This assumption actually reduces the oxide-interface charge distribution given in Fig. 2 to a locally uniform profile for the linear operation region. The benefit of using the triangular charge distribution profile will be demonstrated for the saturation region in sub-section B. A uniform charge distribution profile in the damaged region implies that the channel electron mobility in this region (μ_{n2}) is independent of y and that Q_n is only a function of V_C. Under these simplifying assumptions, the solution of Eq. (11) can be found in two adjacent channel regions.

The parameters associated with the undamaged region (Region 1) and the damaged region (Region 2) will be indicated below with the subscript indices 1 and 2, respectively. Integrating both sides of Eq. (11) from the source to the boundary of the damaged region (L_1) yields

$$I_D \int_0^{L_1} dy = -W \int_0^{V_P} \mu_n(y)\, Q_n(y)\, dV_C \tag{12}$$

$$= W\mu_{n1}C_{ox} \int_0^{V_P} \left[V_G - V_{FB1} - 2|\Phi_P| - V_C - \frac{1}{C_{ox}} \left[2\varepsilon_S q N_a (2|\Phi_P| + V_C - V_B) \right]^{\frac{1}{2}} \right] dV_C \,.$$

$$I_D = \frac{W}{L_1}\mu_{n1}C_{ox} \left\{ (V_G - V_{FB1} - 2|\Phi_P|)\, V_P - \frac{V_P^2}{2} \right.$$

$$\left. - \frac{2}{3} \frac{\sqrt{2\varepsilon_S q N_a}}{C_{ox}} \left[(2|\Phi_P| - V_B + V_P)^{\frac{3}{2}} - (2|\Phi_P| - V_B)^{\frac{3}{2}} \right] \right\} \tag{13}$$

In Eqs. (12) and (13), V_P represents the channel voltage at the boundary of the damaged region, i.e., at $y=L_1$. It is easily seen that Eq. (13) corresponds to the exact drain current equation of an undamaged transistor with channel length L_1 and drain voltage V_P. Since the value of V_P is not known yet, Eq. (11) must now be solved in the damaged region with the corresponding boundary conditions. The integration from the boundary of the damaged region ($y=L_1$) to the drain is carried out as follows.

$$I_D \int_{L_1}^{L} dy = -W \int_{V_P}^{V_D} \mu_n(y)\, Q_n(y)\, dV_C \tag{14}$$

$$= W\mu_{n2}C_{ox} \int_{V_P}^{V_D} \left[V_G - V_{FB2} - 2|\Phi_P| - V_C - \frac{1}{C_{ox}} \left[2\varepsilon_S q N_a (2|\Phi_P| + V_C - V_B) \right]^{\frac{1}{2}} \right] dV_C$$

$$I_D = \frac{W}{L_2}\mu_{n2}C_{ox}\left\{(V_G - V_{FB2} - 2|\Phi_P|)(V_D - V_P) - \frac{1}{2}(V_D^2 - V_P^2)\right. \tag{15}$$

$$\left. - \frac{2}{3}\frac{\sqrt{2\varepsilon_S q N_a}}{C_{ox}}\left[(2|\Phi_P| - V_B + V_D)^{\frac{3}{2}} - (2|\Phi_P| - V_B + V_P)^{\frac{3}{2}}\right]\right\}$$

With some simple manipulation, Eq.(15) can be written in the following form.

$$I_D = \frac{W}{L_2}\mu_{n2}C_{ox}\left\{\left[(V_G - V_P) - V_{FB2} - 2|\Phi_P|\right](V_D - V_P) - \frac{(V_D - V_P)^2}{2}\right.$$

$$\left. - \frac{2}{3}\frac{\sqrt{2\varepsilon_S q N_a}}{C_{ox}}\left[\left\{2|\Phi_P| - (V_B - V_P) + (V_D - V_P)\right\}^{\frac{3}{2}} - \left\{2|\Phi_P| - (V_B - V_P)\right\}^{\frac{3}{2}}\right]\right\} \tag{16}$$

Upon inspection, Eq. (16) can be identified as the exact drain current equation of an nMOS transistor with channel length L_2, drain bias V_D and source bias V_P. Thus, the operation of the damaged nMOS transistor in the linear region is represented by two transistors connected in series. The drain current value I_D for given V_G, V_D and V_B can be obtained by solving Eqs. (13) and (15) with Newton-Raphson iteration. The onset of conduction in the channel is also determined iteratively, since the threshold voltage of the locally damaged nMOS transistor cannot be represented by a closed-form expression. However, the following empirical approximation for the threshold voltage has been found to be sufficiently accurate.

$$V_{Th} = V_{FB2} + 2|\Phi_P| + \frac{\sqrt{2\varepsilon_S q N_a}}{C_{ox}}\sqrt{2|\Phi_P| - V_B}. \tag{17}$$

Here, V_{FB2} represents the *average* flat-band voltage of the damaged channel region.

B. Saturation Region Equations

The analysis leading to the current equations (13) and (15) is valid as long as the inversion charge exists along the entire length of the channel. When the drain voltage V_D is increased sufficiently to cause the mobile electron charge $Q_n(L)$ at the drain to decrease to zero, the channel pinches off and the drain current saturates. Notice that this definition of

current saturation does not take into account the channel velocity saturation effect which dictates the saturation conditions in short channel transistors, and should therefore be viewed as a first-order approximation. The modifications according to channel velocity limitations will be covered in the next section.

The drain voltage corresponding to the onset of saturation can be obtained by setting $Q_n(L) = 0$ in Eq.(9) and solving for $V_C(L) = V_{DSAT}$.

$$V_{DSAT} = V_G - V_{FB}(L) - 2|\Phi_p| + \frac{\varepsilon_S q N_a}{C_{ox}^2}\left\{1 - \sqrt{1 + \frac{2C_{ox}^2}{\varepsilon_S q N_a}(V_G - V_{FB}(L) - V_B)}\right\} \qquad (18)$$

Note that the flat-band voltage V_{FB} in Eq.(18) is calculated using the triangular oxide charge distribution profile, and not the average value of the oxide charge in the damaged region. As the drain voltage V_D is increased beyond V_{DSAT} while the gate voltage is held constant, the effective channel length, i.e., the portion of the channel along which surface inversion exists, decreases due to *channel length modulation*. In the damaged transistor model presented here, the channel-end voltage V_{CE} beyond saturation is calculated by taking into account the non-uniform oxide charge distribution given in Eq.(5). Thus, contrary to the conventional model of the undamaged nMOS transistor in saturation, the channel-end voltage does not remain equal to V_{DSAT} but *increases* as the pinch-off point moves toward the source. For $V_D > V_{DSAT}$, the saturation drain current of the transistor is found by solving Eqs. (13) and (15), where the drain voltage V_D in the equations is replaced by the channel-end voltage V_{CE}.

The length of the depletion region between the drain and the channel-end point is calculated by combining the lateral electric field components due to (i) the potential difference between the drain and channel-end point, (ii) the fringing electric field between the gate and the drain, and (iii) the fringing electric field between the gate and the channel-end point. An approximate formula for the length ΔL of channel-end depletion region has been given by Frohman-Bentchkowsky and Grove [14]. The formula is modified according to the non-

uniform oxide charge distribution as follows.

$$\frac{1}{\Delta L} = \sqrt{\frac{q\,N_a}{2\varepsilon_S\,[V_D - V_{CE}(\Delta L)]}} + \frac{\varepsilon_0}{\varepsilon_S t_{ox}}\,\frac{\alpha\,[V_D - V_G'] + \beta\,[V_G^{\bullet}(\Delta L) - V_{CE}(\Delta L)]}{V_D - V_{CE}(\Delta L)} \tag{19}$$

where

$$V_{CE}(\Delta L) = V_G - V_{FB}(\Delta L) - 2|\Phi_P| + \frac{\varepsilon_S q N_a}{C_{ox}^2}\left\{1 - \sqrt{1 + \frac{2C_{ox}^2}{\varepsilon_S q N_a}(V_G - V_{FB}(\Delta L) - V_B)}\right\} \tag{20}$$

$$V_G^{\bullet}(\Delta L) = V_G - \frac{1}{C_{ox}}\left[Q_{it}(L - \Delta L) - Q_{ox}\right] \tag{21}$$

$$V_G' = V_G - \frac{1}{C_{ox}}\left[Q_{peak} - Q_{ox}\right] \quad . \tag{22}$$

The coefficients α and β represent fringing field factors accounting for the lateral contributions of the fringing electric fields. The channel-end depletion region length ΔL for given bias conditions is calculated from Eqs. (19)-(22) by Newton-Raphson iteration. Thus the nMOS transistor operating in saturation region can be accurately modeled by a transistor with effective channel length $L - \Delta L$ and with the corresponding drain voltage $V_{CE}(\Delta L)$. Linear region current equations (13) and (15) are used to compute the drain current since this modified transistor operates at the saturation boundary. Note that the average oxide charge density used in Eqs. (13) and (15) decreases as the pinch-off point moves away from the drain, because the oxide charge profile directly above the channel-end depletion region has no effect on the drain current. When the length ΔL of the depletion region exceeds the length L_2 of the damaged oxide region, the drain current of the damaged transistor becomes approximately equal to the drain current of an undamaged transistor in saturation.

C. Consideration of Channel Velocity Limitations

The mobile electron charge Q_n moves in the channel under the influence of E_y, the electric field component tangential to the silicon-oxide interface. At the same time, Q_n is held near the interface by the field component E_x, which is perpendicular to it. Both field

components E_x and E_y influence the velocity of the electrons moving along the channel.

Experiments have shown that carrier velocities near the surface tend to saturate at higher tangential fields [15],[23]. This behavior can be modeled by the following expression

$$v = \frac{|\mu_n E_y|}{(1 + |E_y/E_c|^{\alpha})^{1/\alpha}} \tag{23}$$

where v represents the carrier velocity, and α and E_c are empirical parameters. This expression can be further simplified by assuming $\alpha = 1$ [16]. Using Eq. (23) with $\alpha = 1$ and $E_y = -dV_C/dy$, Eq. (11) can be rewritten as

$$I_D = -\frac{\mu_n E_y W Q_n(y)}{1 + (E_y/E_c)} \quad . \tag{24}$$

This equation is reorganized and integrated along the channel to yield:

$$I_D = -\frac{W}{L\,(1 + |V_D/E_c|)} \int_0^{V_D} \mu_n Q_n \, dV_C \quad . \tag{25}$$

Thus the influence of channel velocity saturation can be interpreted as a lengthening of the channel by $|V_D/E_c|$, or as a reduction of the electron mobility μ_n while the channel length is kept constant.

To approximate the drain voltage V_{DSAT} at the onset of saturation, the following semi-empirical expression has been used.

$$V_{DSAT}(new) = \gamma\,|E_c L| \left[\sqrt{1 + \frac{2\,V_{DSAT}}{|E_c L|}} - 1\right] \tag{26}$$

Here, the coefficient γ with a value between 0.9 and 1.0 accounts for the fact that the channel actually saturates *before* the mobile electron charge Q_n is reduced to zero at the drain.

In addition to the effects of channel velocity saturation, the influence of the vertical electric field E_x upon carrier transport must also be considered. This field component influences the scattering at the silicon-oxide interface, and causes a virtual reduction of the carrier mobility in the channel [15]. This effect, combined with the carrier velocity saturation examined

above, has been modeled empirically as

$$\mu_{eff} = \frac{\mu_n}{1 + |V_D/E_cL| + \eta V_G} \quad . \tag{27}$$

In this expression, E_c represents the characteristic field for the channel velocity, and η represents the empirical parameter corresponding to the vertical field effect. Equation (27) can be used for both regions of the damaged MOSFET; by setting the drain voltage equal to V_P in the undamaged Region I, and $V_D - V_P$ in the damaged Region II. With this simple improvement, the proposed MOSFET model accurately simulates the behavior of transistors with channel lengths down to 1 μm.

D. Pseudo Two-Dimensional Modeling of Damaged MOSFETs

The one-dimensional model equations in this section were derived using the assumption that the gradual channel approximation is valid for the damaged nMOS transistor, and in particular, for the short damaged region at the drain end of the channel. However, this assumption becomes questionable for transistors with very short channels, i.e., for sub-micron geometries, where the potential distribution becomes two-dimensional. Thus, the calculation of the depletion region length and the saturation voltage requires the accurate estimation of the vertical as well as the horizontal electric field components in the drain region using a pseudo two-dimensional modeling approach [17],[18].

When the nMOS transistor is operating in saturation, the channel is divided into two regions: The source region where the Gradual Channel Approximation (GCA) is valid, extending from the source to the point of saturation, and the drain region extending from the point of saturation to the drain junction. The saturation current can be found by setting the channel-end voltage equal to V_{DSAT} and channel length equal to $L - \Delta L$ in the linear region equations, and solving for I_D. Thus, the drain depletion region length ΔL and the saturation voltage V_{DSAT} must be determined using the pseudo two-dimensional analysis. In the drain region, mobile electrons are assumed to spread over an average depth X_{av}. A rectangular

Gaussian surface that encloses both the mobile and bulk charges is shown in Fig. 3. Applying Gauss's law to the sides of the rectangle yields the following expression.

$$-\int_0^{x_w} \varepsilon_s E_1 \, dx + \int_0^{y} \varepsilon_s E_2 \, dy + \int_0^{x_w} \varepsilon_s E_3 \, dx - \int_0^{y} \varepsilon_{ox} E_4 \, dy = -q \int_0^{y} \left[\int_0^{x_w} (n + N_A) \, dx \right] dy \tag{28}$$

Here, E_1, E_2, E_3 and E_4 are the electric fields perpendicular to the boundaries of the Gaussian surface. Note that the field component E_4, which represents the oxide electric field above the drain depletion region, also contains the contribution of the localized oxide charge due to hot-carrier damage. An approximate solution of Eq. (28) can provide the saturation voltage V_{DSAT} as well as the depletion region length ΔL as a function of the external bias conditions [18],[19]. However, this approach still requires a simultaneous solution of five non-linear equations, which significantly increases the computational complexity of the model and diminishes its applicability for circuit-level simulation tasks.

E. Simulation Results

The accuracy and various properties of the damaged MOSFET current model will be examined by comparing the simulation results with experimental data. Circuit simulation examples will also be presented to indicate the implementation of the new model for simulating hot-carrier induced circuit performance degradation.

The measured and simulated I_D–V_D characteristics of an nMOS transistor before and after hot-carrier stress are given in Fig. 4. The experimental data on the damaged nMOS transistor were obtained from Texas Instruments, Inc. The geometry of the measured nMOS transistor is described by the following parameters: W = 10 μm, L = 1.0 μm, t_{ox} = 20 nm. The transistor has been stressed under maximum hot-carrier injection conditions (V_D = 6.5 V, V_G = 2.6 V) for 423 hours. The simulated I_D–V_D characteristics correspond to a peak interface charge density of $Q_{peak} = q \cdot 8.2 \times 10^{11}$ C/cm^2 and to a damaged region length of $L_2 = 0.12$ μm. The model

parameters which had not been specified by the device manufacturer were optimized using the parameter extraction routine in iSMILE. A list of model parameters and their values are given in Table 1.

The comparison with the measurement results demonstrates that the proposed model is capable of accurately representing the behavior of the nMOS transistor after localized hot-carrier damage. Figure 5 shows the measured and the simulated output conductance of the undamaged transistor. For accurate circuit reliability simulation, the transistor model must be able to represent the behavior of the damaged device for different hot-carrier damage levels, which correspond to different stress times under DC conditions. In Figure 6, the measured drain current degradation versus hot-carrier stress time is compared with simulation results. The drain current degradation is defined as the decrease of the current at $V_G = 5$ V, $V_D = 1.5$ V. The DC stress conditions are $V_D = 6.5$ V, $V_G = 2.6$ V.

The forward and reverse I_D–V_D characteristics of a damaged nMOS transistor are given in Fig. 7 [7]. In this example, the channel length of the transistor is L = 1.7 μm, and the stress conditions are $V_D = 8$ V, $V_G = 3$ V, $t_{stress} = 5 \times 10^4$ s. The proposed MOSFET model replicates the strong asymmetry between forward and reverse operation, which is due to the localization of oxide-interface damage near the drain. The uniform charge distribution model [2],[5] is not capable of reproducing this asymmetry which may seriously affect the performance of bidirectional devices such as transmission gates. On the other hand, the uniform model was found to provide satisfactory simulation results for the case where both the source and drain ends of the channel are subjected to equal amounts of hot-carrier damage. Figure 8 shows the simulated I_D–V_G characteristics of an nMOS transistor with different levels of hot-carrier damage. As expected, the threshold voltage increases with the amount of oxide-interface charge. Notice that the maximum channel transconductance also increases as a result of localized degradation. This phenomenon, which was also observed in two-dimensional device simulations with PISCES using *fixed* negative oxide charges in the drain region [8], is due to the ini-

tial model assumption that all generated interface traps are occupied with electrons.

The circuit-level implementation of the proposed MOSFET model using the iSMILE circuit simulator is demonstrated in the next example. A 7-stage CMOS ring oscillator with 0.2 pF loading at each stage is considered. The (W/L)-ratios of the nMOS and pMOS transistors are (10/2) and (15/2), respectively. To investigate the influence of hot-carrier induced device damage upon the circuit performance, a localized oxide-interface charge ($Q_{peak} = q \cdot 1.5 \times 10^{12}$ C/cm^2, $L_2 = 0.1$ μm) is introduced in all nMOS transistors, and the circuit is simulated with iSMILE. Figure 9 shows a degradation (decrease) of the ring oscillator frequency by approximately 10% due to the localized oxide damage in nMOS transistors. To compare this result with uniform-damage model results, the same amount of interface charge is assumed to be distributed uniformly along the channel region of each transistor, and the circuit is simulated with iSMILE. It is found that the observed degradation of the oscillation frequency is about 5%, indicating that a transistor model based on uniform charge distribution tends to underestimate the circuit performance degradation. The simulated operation of a cross-coupled latch circuit is shown in Fig. 10 with (i) locally damaged transistors, and (ii) uniformly damaged transistors. As in the previous example, it can be seen that the uniform-damage assumption again underestimates the circuit performance degradation. The rise time and the fall time of the respective terminal voltages after degradation are found to be significantly larger using the localized damage model.

Finally, the hot-carrier induced degradation of an nMOS transistor in bidirectional operation is examined in the following example. Figure 11 shows a simple nMOS pass-transistor structure in which the capacitances C_1 and C_2 are charged and discharged during each cycle. The pass-transistor M3 experiences significantly more hot-carrier degradation during the *charge* phase than during the *discharge* phase because the initial drain-to-source voltage is higher in the former case. Consequently, transistor M3 is expected to sustain a unidirectional oxide damage despite of its bidirectional operation mode. The result of this one-sided local

damage is that the drain current is significantly reduced during the *discharge* phase, since the oxide damage is then located at the source end of the channel. The simulated input and output voltage waveforms are shown in Figure 12. It is seen that the fall time of the output voltage waveform increases with hot-carrier induced damage, because the drain current of M3 during discharge phase is substantially reduced.

IV. Reliability Simulation of Very Large CMOS Circuits

In the previous section, we have presented a new approach for simulating hot-carrier induced MOS circuit degradation. However, the detailed circuit simulation needed for determining the stress conditions of individual devices restricts the computational efficiency of reliability simulation approaches for very-large scale integrated circuits.

Figure 13 shows a hierarchical simulation approach presented for estimating the hot-carrier induced degradation of device characteristics and circuit performance in large scale MOS circuits. The reliability simulation tool presented here incorporates a two-tier hierarchical simulation approach for improving the computational efficiency. Large circuits are simulated using a fast timing simulator to detect subcircuits likely to cause reliability problems. Then, detailed circuit simulation is performed on the suspected subcircuits. An accurate one-dimensional MOSFET model and a repetitive simulation scheme are adopted to ensure accurate prediction of the circuit-level degradation process under dynamic operating conditions. The fast simulation is performed using the mixed-mode simulator iDSIM2, whereas iSMILE is used for the detailed simulation [24].

iDSIM2 reads in a SPICE-type circuit description and creates a circuit database. Based on this database, iDSIM2 performs the following preprocessing. First, it partitions the MOS circuit into channel-connected subcircuits and adds the information back to the database. Each subcircuit may contain transistors, resistors, diodes and capacitors. It detects feedback loops existing in the circuit based on the basic principle that signals propagate from gate node to drain and source nodes of a MOS transistor while the signal propagation between drain and

source is bi-directional. iDSIM2 also detects subcircuits which have the same circuit configuration and builds a two-level hierarchy. Although iDSIM2 also includes other higher level simulation options such as switch-level and logic-level simulation, only circuit and fast-timing are involved in reliability analysis because of the accuracy requirements.

The use of the device degradation models must be restricted to shorter time intervals in which the change of stress conditions may be neglected. It is assumed that the degradation model can be applied to predict the hot-carrier induced device degradation accurately within a time interval of length T_1. The goal is to predict the amount of device and circuit performance degradation for the operation time interval $T_2 > T_1$. The period, T_0, of the input waveform is assumed to be $T_0 \ll T_1, T_2$.

Simulation procedure :

(i) Simulate the circuit for one period (T_0) and determine the stress conditions (terminal voltage waveforms) associated with each nMOS transistor.

(ii) Using the hot-carrier degradation models, determine the amount of degradation that each transistor will experience at the end of the time interval T_1.

(iii) Update the damage parameters of each transistor to specify the hot-carrier degradation sustained at the end of T_1.

(iv) Return to (i) and repeat the procedure k times such that $T_2 = k\ T_1$.

It can be seen that the results of each circuit simulation cycle (for one period T_0) are used to estimate the amount of hot-carrier induced damage each transistor will experience during a time interval of length T_1.

After each one-cycle simulation, the damage level of each transistor is extrapolated to the previously specified time period, and the parameters are updated accordingly. Based on this

information, the user may want to switch those subcircuits which have no degradation to fast-timing in order to increase speed. The user can also change the operation duration if the previous one is too long or too short, and re-run the simulation. With this mixed-mode simulation capability, iDSIM2 can handle large circuits with computational efficiency.

The use of macromodels is also being considered for representing damaged subcircuits in circuit-level simulation using iDSIM2. This, combined with the use of fast-timing macromodels for undamaged subcircuits, will further improve the computational efficiency while preserving the required accuracy.

A 824-transistor combinational circuit has been simulated to demonstrate the large-scale simulation capability of iDSIM2. The simulation cycle length in this example is $T_0 = 84$ ns. Following the one-cycle simulation, hot-carrier induced degradation of the nMOS transistors are estimated for time interval of $T_1 = 5\times10^6$ seconds. After updating the damage parameters, the simulation is repeated as described earlier. The total CPU time for performing this simulation on a Sun 3/160 is 48 minutes. The distribution of the simulated hot-carrier damage levels in nMOS transistors is given in Fig. 14. The second peak of the distribution graph indicates the transistors with extensive hot-carrier induced damage, which can influence the circuit performance characteristics. Thus, any gate containing at least one extensively damaged transistor must be classified as a "damaged gate."

V. Design of Reliability Tester

The reliability simulation tools developed in this task need to be verified and calibrated using experimental data on hot-carrier degradation of MOS circuits under realistic operating conditions. To achieve this goal, a tester chip containing a 42-stage inverter chain has been designed at the University of Illinois, and fabricated by Sematech in the 1990-1991 period. In the tester chip, some transistors have been designed to be individually controllable and observable, for accurate determination of device characteristics before and after hot-carrier stress. The circuit can be stressed under different dynamic operating conditions for different

lengths of operation. The changes in the transistor characteristics can be monitored at certain intervals during long-term stressing in order to determine the amount of hot-carrier stress experienced by each device.

The transistors to be accessed externally are organized into two separate test cells, each of which contains two CMOS inverters in series. The first test cell constitutes stage 15 and stage 16 of the inverter chain, whereas the second test cell constitutes stage 31 and stage 32. Except for the test cells, the (W/L)-ratios of nMOS and pMOS transistors are (14.4/1.2) and (29.4/1.2), respectively. The test cells contain one inverter with the same (W/L)-ratios as the regular stages, and one inverter with (W/L)-ratios of (9.6/1.2) and (14.4/1.2). Two versions of the test chip have been manufactured using the Phase-2 and Phase-3 design rules developed by Sematech.

As indicated on the test-cell circuit diagram in Fig. 15, 8 pads are dedicated to each test cell so that all four transistors in a cell are independently accessible. This feature allows the accurate measurement of device model parameters of each transistor under various bias conditions, before and after hot-carrier stress. The transistors in the test cells can be stressed under dynamic circuit operating conditions, or under externally applied DC-bias conditions to accelerate the degradation of individual devices. In addition to the 3 pads for Vss and 2 pads for Vdd, one pad each is provided for signal input, 41st stage output and 42nd stage output. The 41st stage output can be used to convert the inverter chain circuit into a ring oscillator by an external connection.

VI. Summary

During the last project period, we have developed new simulation capabilities for reliability analysis of MOS circuits with emphasis on hot-carrier damages. In particular, both iSMILE and iDSIM2 have been used to develop and implement new reliability models of nMOS transistors.

The physical one-dimensional model for hot-carrier damaged nMOS transistor has been shown to explain the unique asymmetry in I-V characteristics due to local damages in the drain of the channel, besides the changes in the transconductance g_m and the mobility degradation. This model can be incorporated in SPICE-like circuit simulators as demonstrated through iSMILE which is a model-independent circuit simulator that enables rapid model development. Simulation results have shown strong agreements with measured data on transistor characteristics, which points to potential matches at circuit level. However, the circuit level simulation capability remains to be verified in the future due to insufficient data.

To extend the circuit simulation capability to large MOS circuits, we have also developed a two-tier mixed-level reliability simulation approach using the iDSIM2 program. Using iDSIM2, we have been able to simulate a 824-transistor combinational circuit on a Sun-3/160 workstation. This is a major speed improvement over iSMILE-based simulation and allows in-depth reliability analysis of large MOS circuits.

In an effort to verify the accuracy of circuit simulation using iSMILE or iDSIM2, we have designed a CMOS tester wherein I-V characteristics of some transistors can be measured individually before and after hot-carrier stress. This tester is being fabricated by Sematech. Future experiments with the fabricated tester chips should be helpful in improving the model and the simulation capability.

Besides the planned experimental verification tasks, other basic tasks need to be investigated. To mention a few, development of models for pMOS transistors and lightly doped drain (LDD) structures would be important in view of technology trends. Furthermore, to cope with the ever-increasing level of device integration, a faster simulator that can handle several hundreds of thousands of transistors needs to be developed.

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PARAMETER	VALUE
W (cm)	10.0×10^{-4}
L (cm)	1.0×10^{-4}
μ_0 (cm^2/V^2s)	678.5
Φ_{MS} (V)	−0.8385
Φ_P (V)	0.354
N_A (cm^{-3})	1.809×10^{15}
N_{ox} (cm^{-3})	1.0×10^{10}
t_{ox} (cm)	224×10^{-8}
α	0.3188
β	0.4982
η	0.0802
E_c (V/cm)	2.36×10^4

Table 1

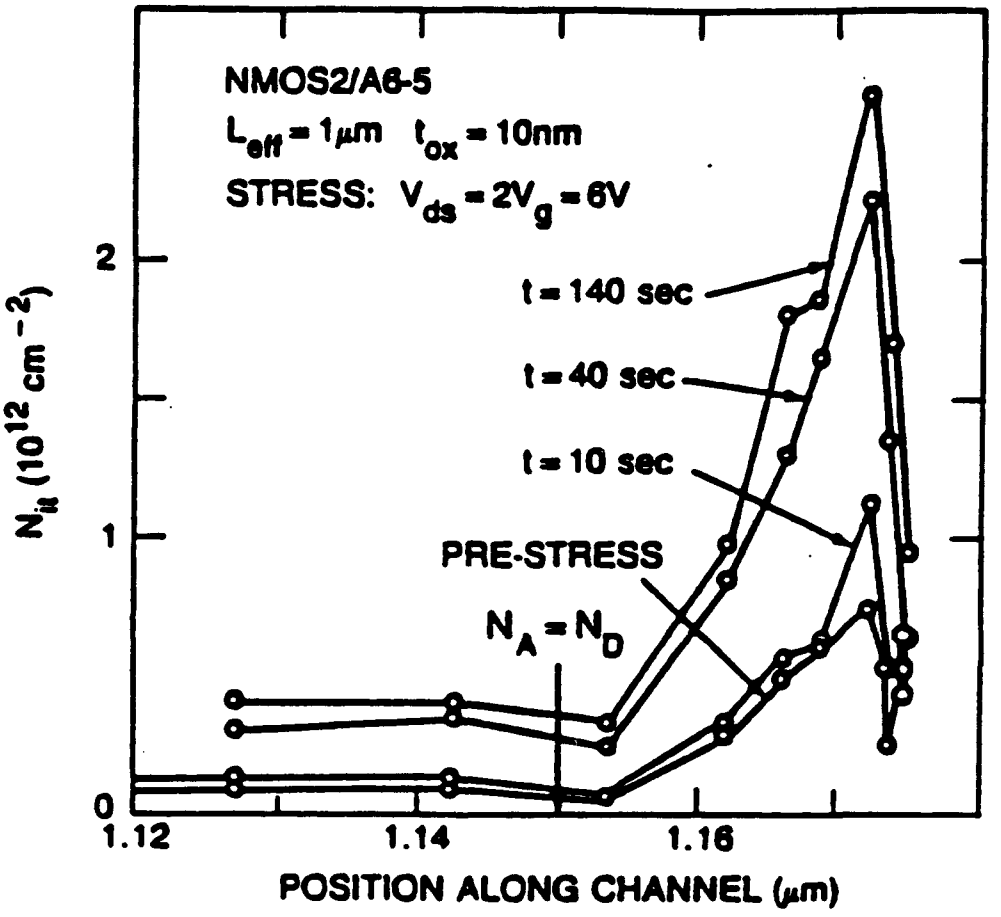


Fig. 1. Measured interface charge distribution profile near drain [12].

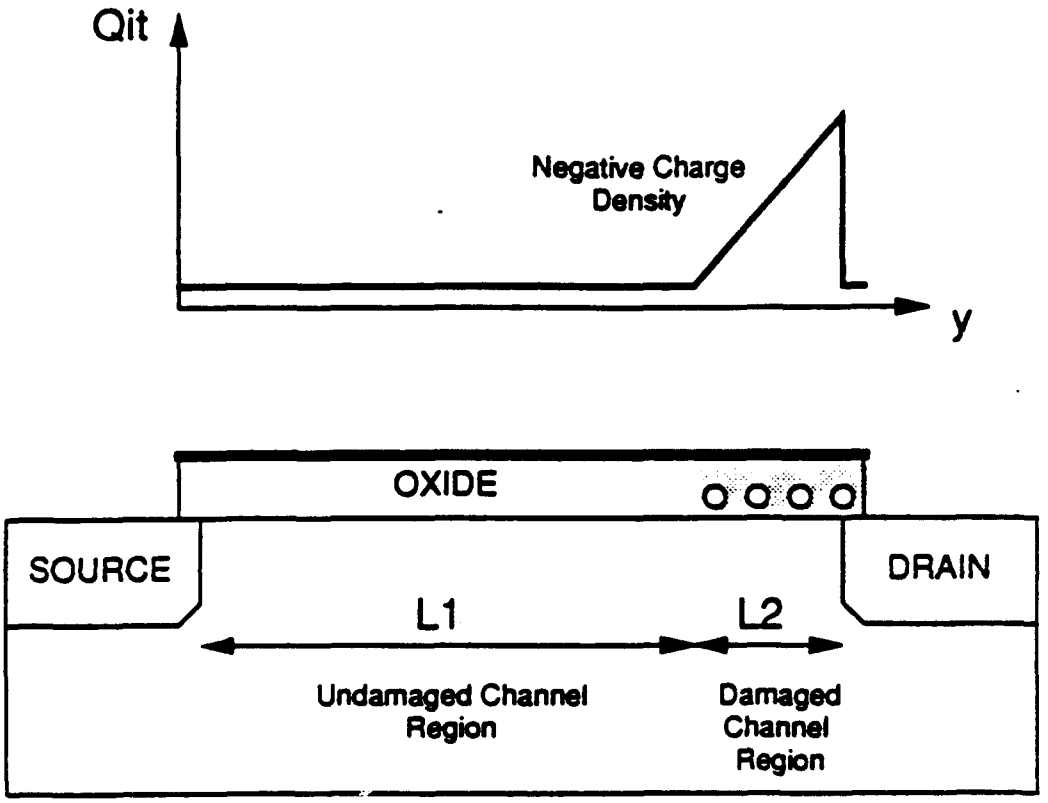
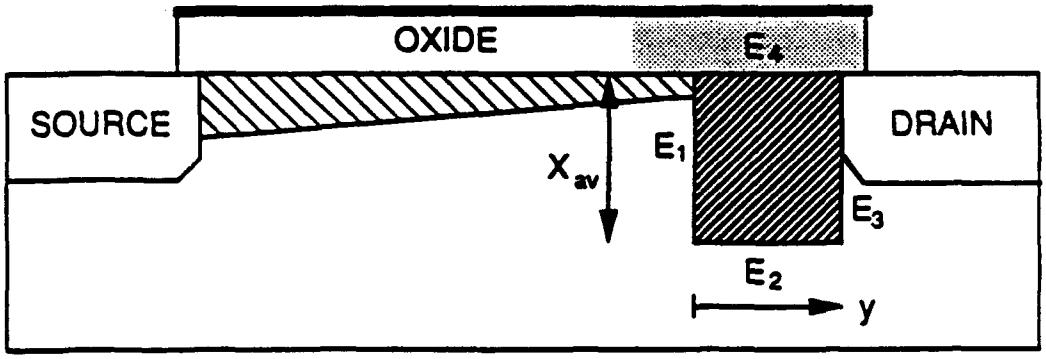


Fig. 2. Oxide charge distribution profile used in model derivation.



Damaged oxide region

Gaussian surface enclosing mobile and bulk charges

Channel region where **GCA** is valid

Fig. 3. Pseudo two-dimensional modeling of the damaged MOSFET.

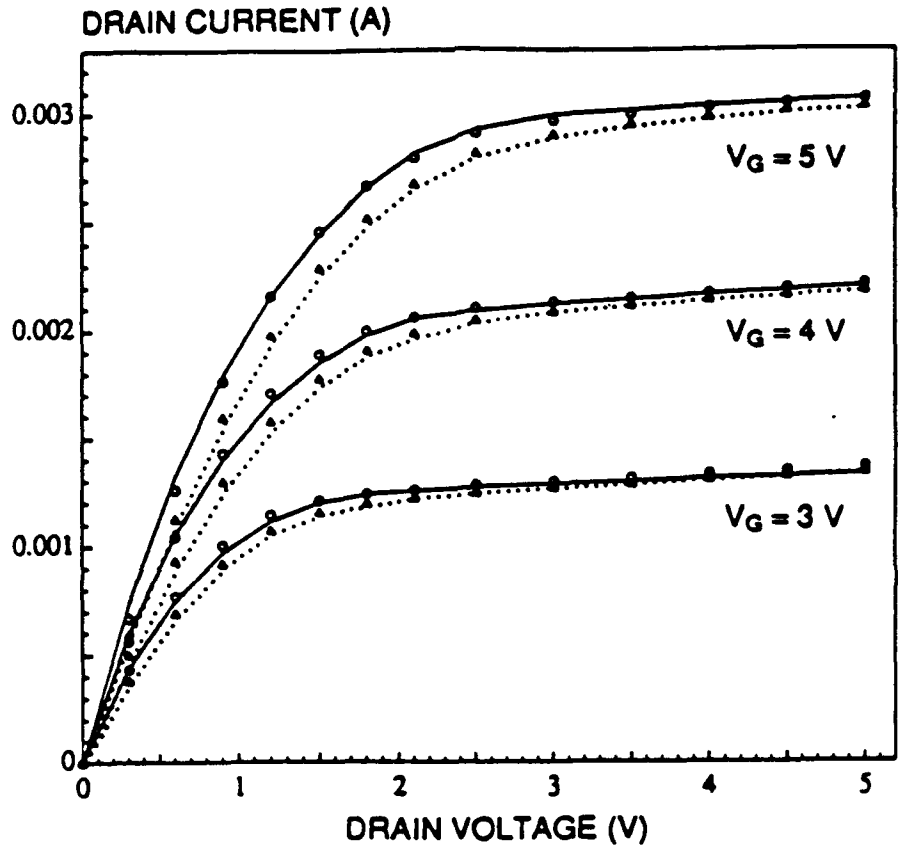


Fig. 4. Comparison of measured and simulated I_D-V_D characteristics of the nMOS transistor before and after hot-carrier stress. Stress conditions : $V_G = 2.6$ V, $V_D = 6.5$ V, $t_{stress} = 423$ h.

O : Measured drain current *before* stress

Δ : Measured drain current *after* stress

Solid lines : Simulated drain current *before* stress

Dotted lines : Simulated drain current *after* stress

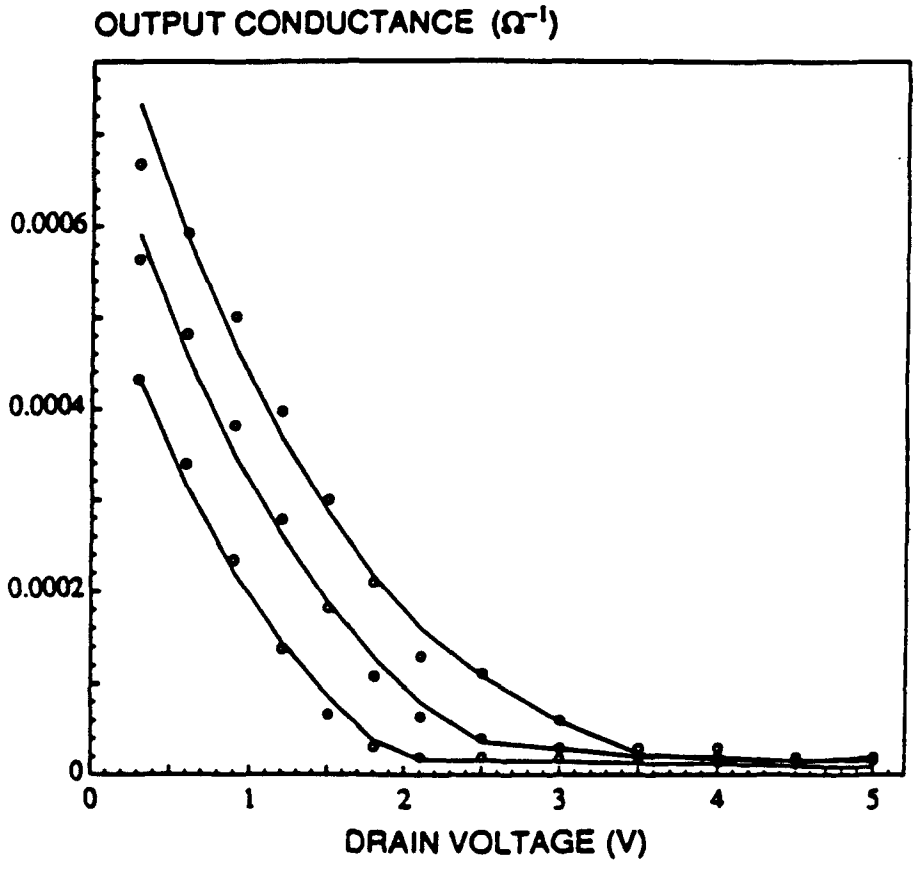


Fig. 5. Measured (circles) and simulated (solid lines) output conductance of the undamaged nMOS transistor.

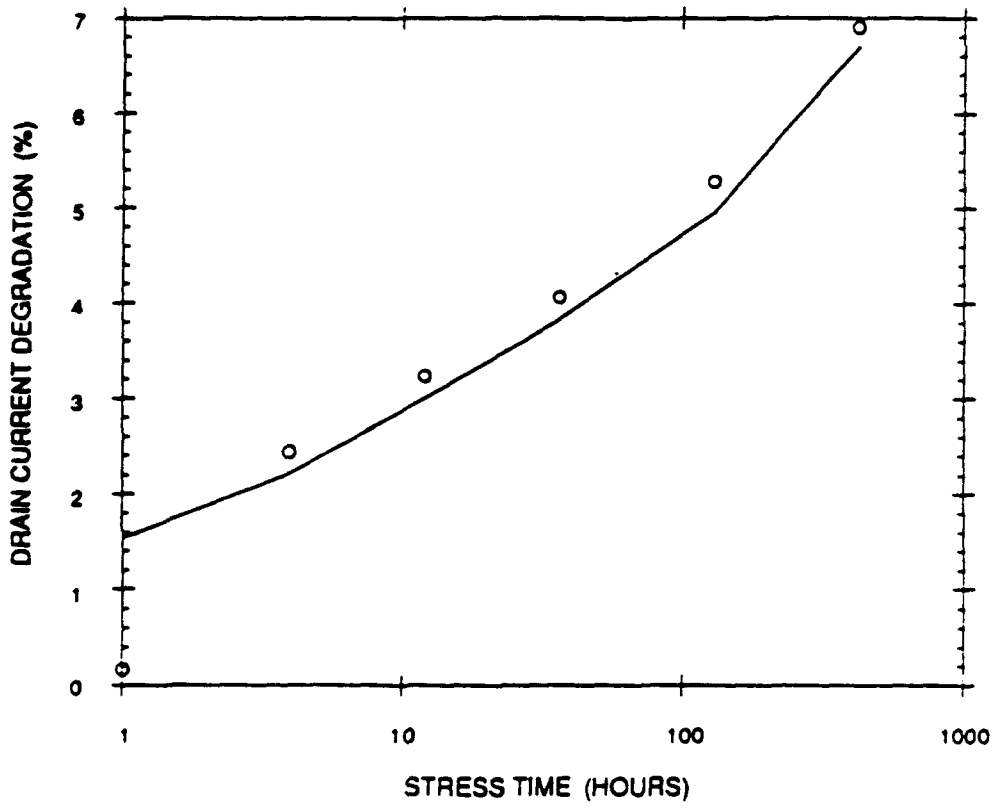


Fig. 6. Measured (circles) and simulated (solid line) drain current degradation as a function of the stress time. Stress conditions : $V_G = 2.6$ V, $V_D = 6.5$ V.

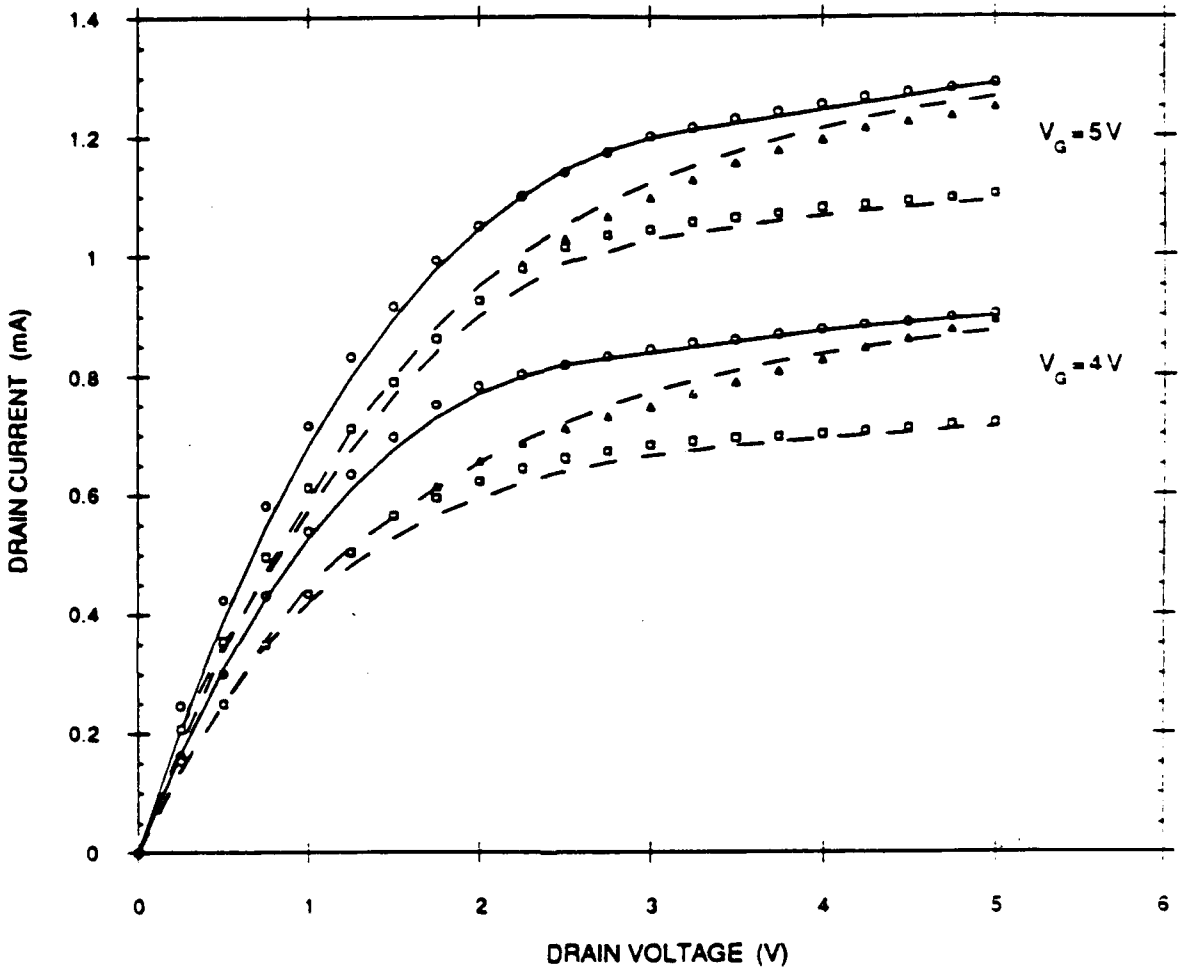


Fig. 7. Forward and reverse I_D–V_D characteristics of the nMOS transistor before and after hot-carrier stress. Stress conditions : $V_G = 3$ V, $V_D = 8$ V, $t_{stress} = 5 \times 10^4$ s. Channel length L = 1.7 μm [7].

○ : Measured (forward and reverse) drain current *before* stress

Δ : Measured forward drain current *after* stress

□ : Measured reverse drain current *after* stress

Solid lines : Simulated drain current *before* stress

Dashed lines : Simulated drain current *after* stress

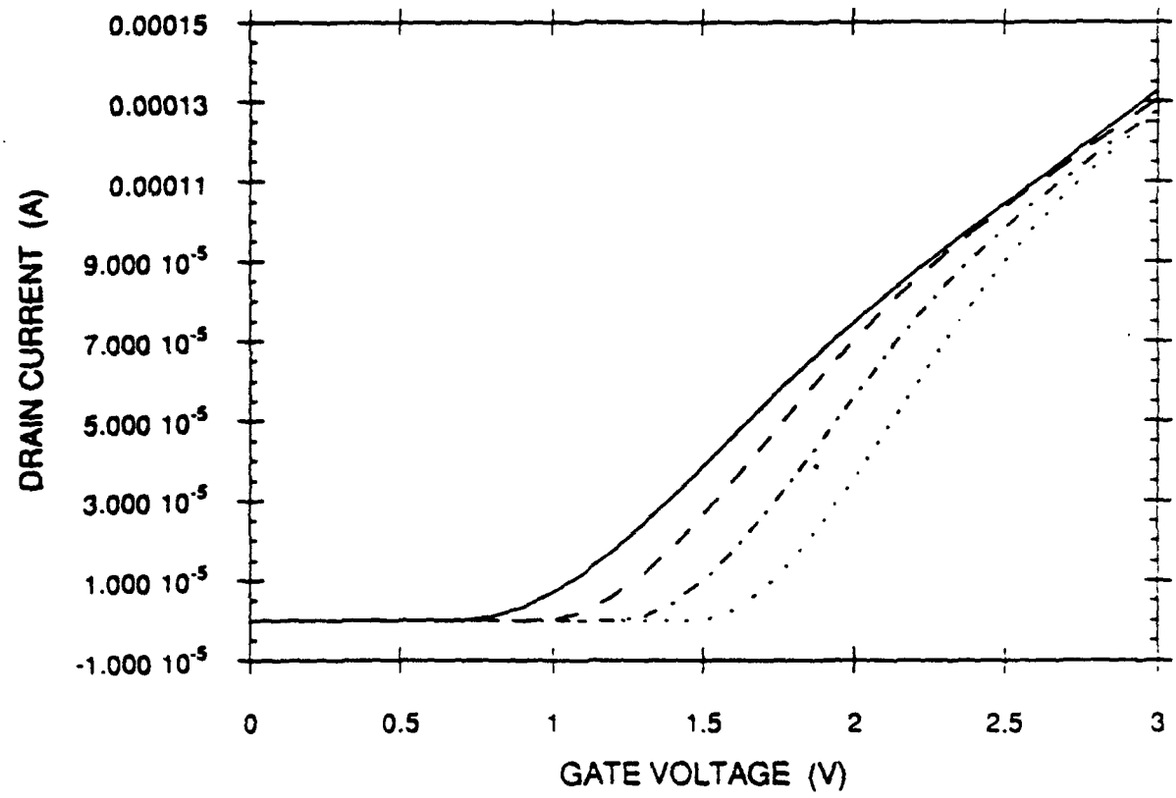


Fig. 8. Simulated I_D–V_G characteristics of the nMOS transistor with different levels of hot-carrier damage N_{it}.

Solid line : Undamaged device ($N_{it} = 0$).

Dashed line : $N_{it} = 0.5\times10^{12}$ cm^{-2}.

Dash-dotted line : $N_{it} = 1.0\times10^{12}$ cm^{-2}.

Dotted line : $N_{it} = 1.5\times10^{12}$ cm^{-2}.

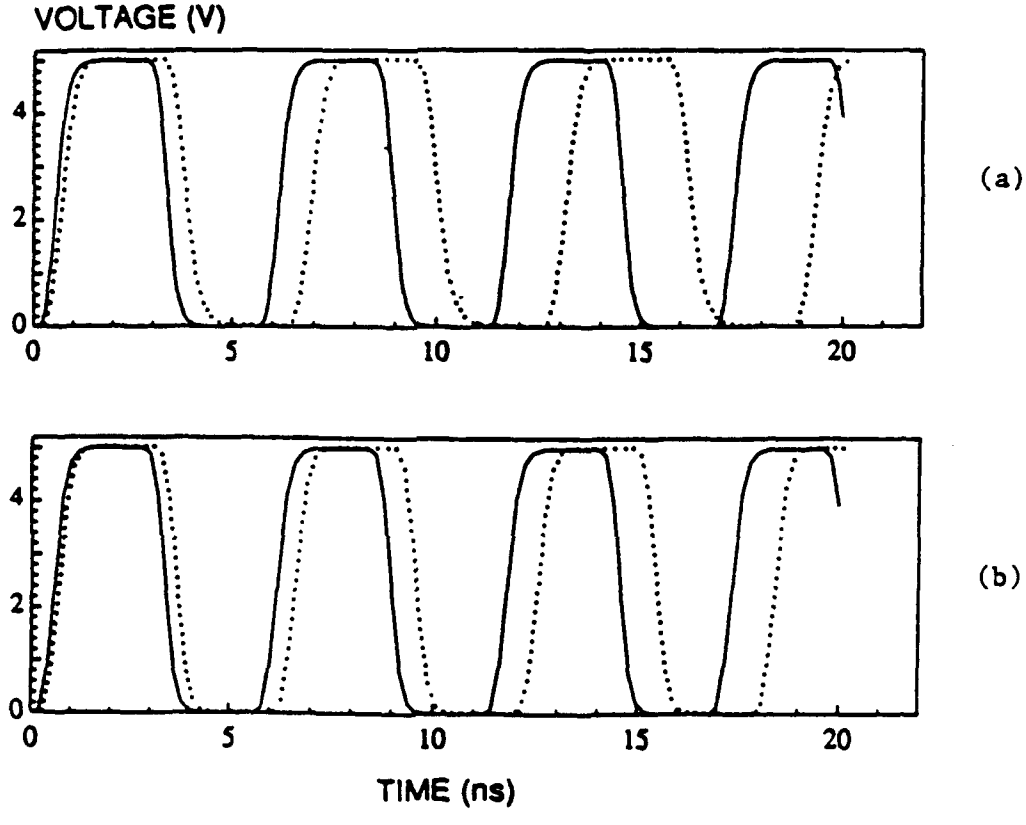


Fig. 9. Simulated operation of the 7-stage ring oscillator before (solid lines) and after (dotted lines) hot-carrier induced oxide damage.

(a) Locally damaged nMOS transistors

(b) Uniformly damaged nMOS transistors

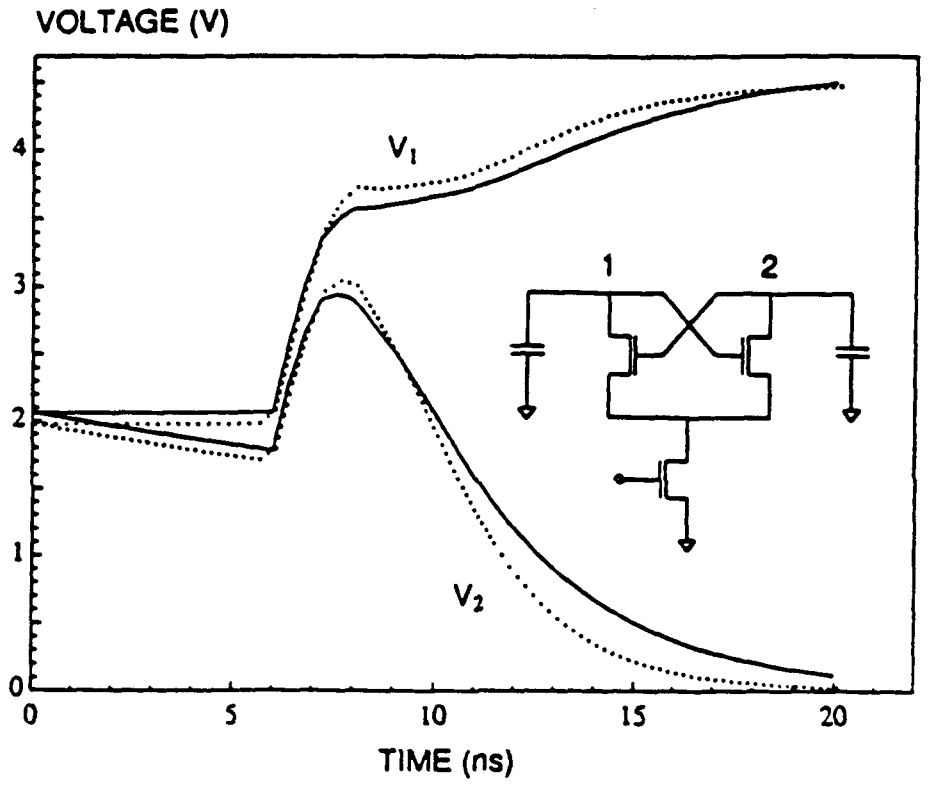


Fig. 10. Simulated operation of the cross-coupled latch circuit (inset), with locally damaged transistors (solid lines) and with uniformly damaged transistors (dotted lines).

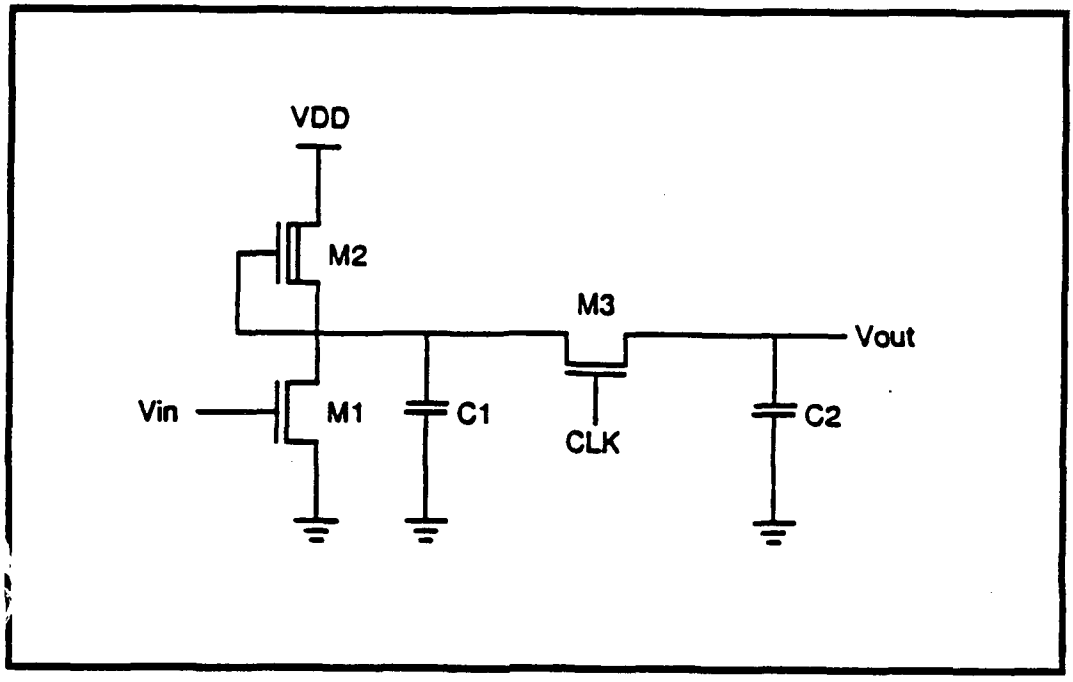


Fig. 11. nMOS Pass-transistor circuit.

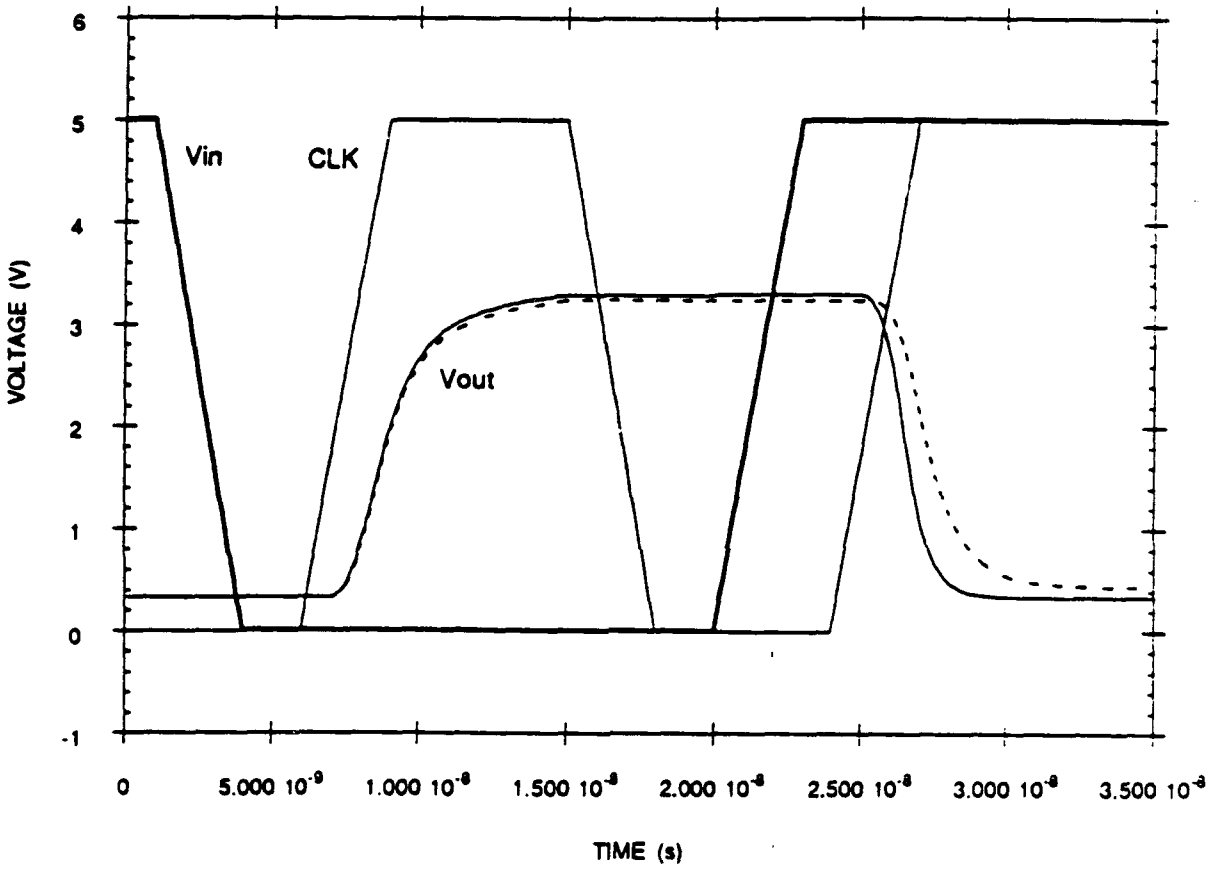


Fig. 12. Simulated input and output voltage waveforms of the nMOS pass-transistor circuit.

Solid line : Before degradation.

Dashed line : After degradation.

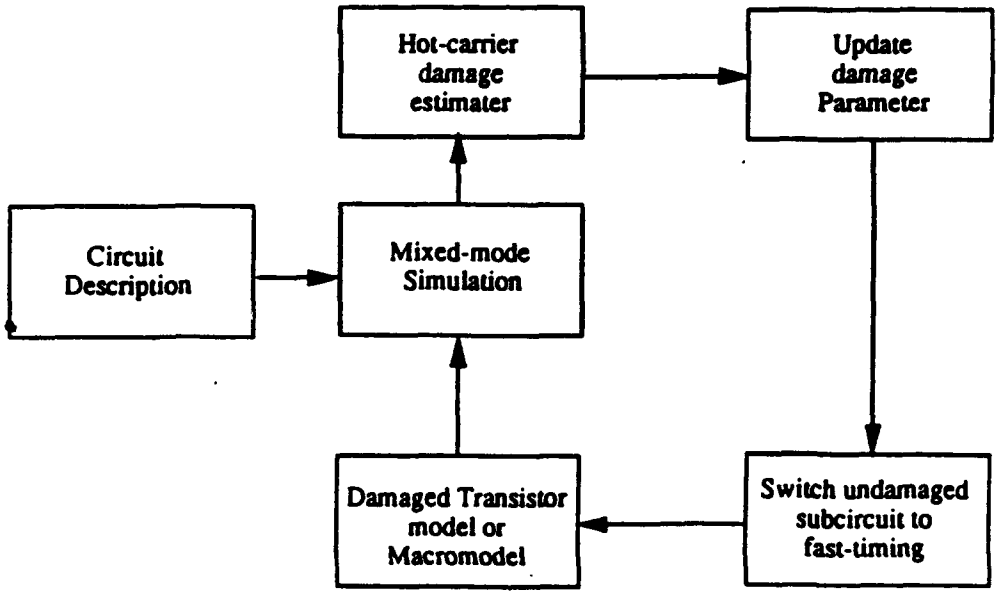


Fig. 13. Structure of the reliability simulation procedure.

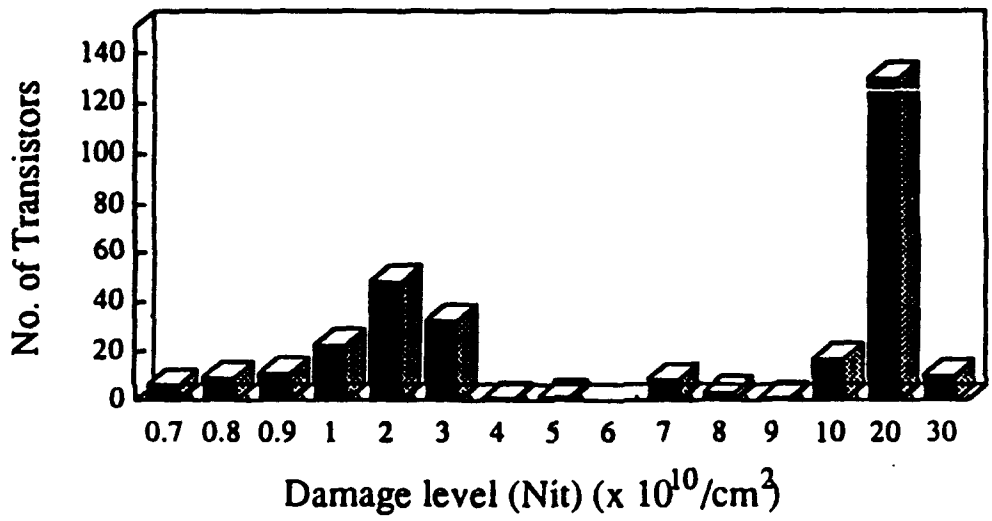


Fig. 14. Distribution of simulated hot-carrier damage levels in nMOS transistors after 5×10^6 seconds of dynamic operation.

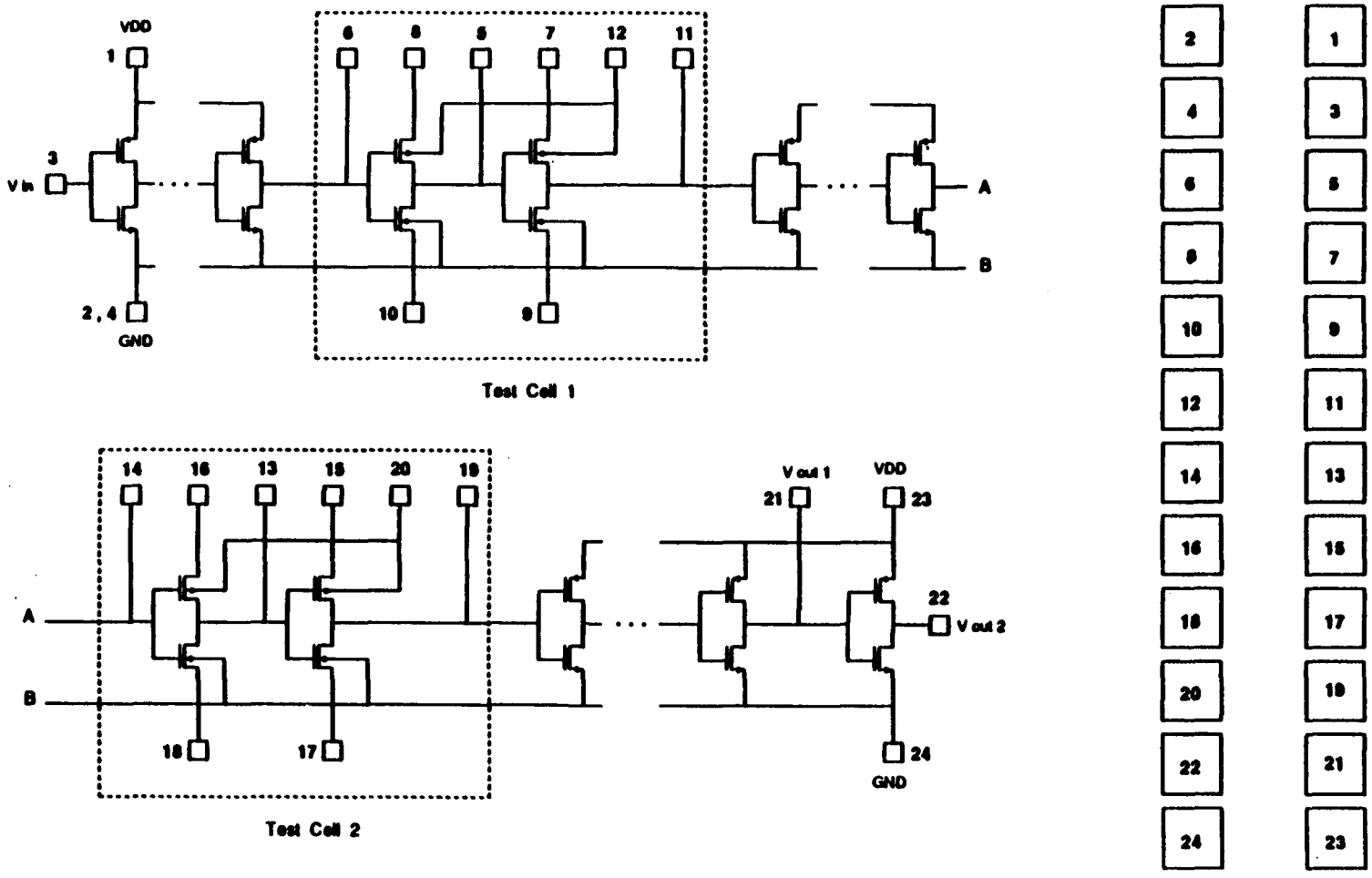


Fig. 15. Circuit diagram of the tester with pad assignments.

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